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CLAIMS

1. A power driver circuit comprising:

a low voltage source;

a high voltage source;

a first input node;

an output node; and

circuitry adapted to connect said output node to said low voltage source when a signal at said first input node is in a first state and to said high voltage source when said signal at said first input node is changed to a second state.

2. The power driver circuit of claim 1, comprising a second input node, wherein said circuitry comprises:

low voltage switching circuitry adapted to connect said output node to said low voltage source when signals at said first and second input nodes are in a low voltage configuration;

high voltage switching circuitry adapted to connect said output node to said high voltage source when signals at said first and second input nodes are in a high voltage configuration; and

ground switching circuitry adapted to connect said output node to ground when signals at said first and second input nodes are in a ground configuration.

3. The power driver circuit of claim 2, wherein said low voltage switching circuitry comprises a first low voltage activation switch activated by said signal at said second input node and a second low voltage activation switch activated by said signal at said first input node
4. The power driver circuit of claim 3, wherein said second low voltage activation switch is an inverted switch
5. The power driver circuit of claim 2, wherein said high voltage switching circuitry comprises a high voltage activation switch activated by said signal at said second input node
6. The power driver circuit of claim 5, wherein said high voltage activation switch is an inverted switch
7. The power driver circuit of claim 2, wherein said ground circuitry comprises a first grounding switch activated by said signal at said first input node and a second grounding switch activated by said signal at said second input node.
8. The power driver circuit of claim 3, wherein said switches are NMOS transistors.
9. The power driver circuit of claim 3, wherein said inverted switches are PMOS transistors.
10. The power driver circuit of claim 3, wherein said inverted switches are CMOS transistors.
11. The power driver circuit of claim 1, wherein said low voltage source is charged during a discharge of said power driver circuit.

12. The power driver circuit of claim 1, wherein said low voltage source is Vcc.

13. A method to drive power from a low voltage source and a high voltage source to an output node, the method comprising:

connecting said output node to said low voltage source when a signal at a first input node is in a first state and to said high voltage source when a signal at said first input node is changed to a second state.

14. The method of claim 13, wherein said connecting said output node to said high voltage source when a signal at said first input node is in said second state comprises providing a high voltage on signal at said first input node to a switch connecting said output node to said low voltage source.

15. The method of claim 13, wherein said connecting said output node to said low voltage source when a signal at said first input node is in said first state comprises providing a low voltage off signal at said first input node to a switch connecting said output node to said low voltage source.

16. The method of claim 13 comprising:

connecting said output node to ground when said signal at said first input node is in said first state and when a signal at a second input node is changed from a first state to a second state.

17. The method of claim 13 comprising:

connecting said output node to said low voltage source after disconnecting said output node from said high voltage source, thereby charging said low voltage source.